Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method for processing a matrix of elements in a processor, the method comprising steps of:

loading a first subset of matrix elements of the matrix from a first location;

loading a second subset of matrix elements of the matrix from a second location;

storing a third subset of matrix elements in a first destination; and

storing a fourth subset of matrix elements in a second destination, wherein:

the loading and storing steps result from a first instruction issue,

at least one of the first and second destination consists of a row or column of a second matrix, and

the second matrix corresponds to a transposition of the matrix.

2. (Previously Presented) The method for processing the matrix of elements in the processor as recited in claim 1, wherein:

a first number of sub-instructions perform a ~~an n-by-n~~ matrix transpose, and

the matrix transpose operates on the matrix that has a number of columns equal to the first number.

3. (Original) The method for processing the matrix of elements in the processor as recited in claim 1, wherein the first loading step is performed with a first processing path and the second loading step is performed with a second processing path.

4. (Original) The method for processing the matrix of elements in the processor as recited in claim 1, further comprising the steps of:

loading a fifth subset of matrix elements from a fifth location;

loading a sixth subset of matrix elements from a sixth location;

storing a seventh subset of matrix elements in a third destination; and

storing a eighth subset of matrix elements in a fourth destination.

5. (Original) The method for processing the matrix of elements in the processor as recited in claim 4, wherein the loading and storing steps introduced in claim 4 result from a second instruction issue.

6. (Original) The method for processing the matrix of elements in the processor as recited in claim 4, wherein each of the first through fourth destination include a matrix column.

7. (Original) The method for processing the matrix of elements in the processor as recited in claim 1, wherein each of the first through fourth locations include a matrix row.

8. (Original) The method for processing the matrix of elements in the processor as recited in claim 1, wherein the third and fourth subsets each comprise elements from the first and second subsets.

9. (Original) A processing core for transposing a matrix, comprising:

a first source location comprising a first plurality of matrix elements;

a second source register comprising a second plurality of matrix elements;

a third source register comprising a third plurality of matrix elements;

a fourth source register comprising a fourth plurality of matrix elements;

a first destination register comprising a fifth plurality of matrix elements;

a second destination register comprising a sixth plurality of matrix elements;

a first processing path coupled to the first through fourth source registers and the first destination register; and

a second processing path coupled to the first through fourth source registers and the second destination register.

10. (Original) The processing core for transposing the matrix of claim 9, wherein:

the first through fourth registers each include a plurality of source fields, and

each source field includes a matrix element.

11. (Original) The processing core for transposing the matrix of claim 9, wherein:

the first and second destination registers each include a plurality of result fields, and

each source field includes a matrix element.

12. (Original) The processing core for transposing the matrix of claim 9, further comprising

first and second instruction processors; and

an exchange path between the first and second instruction processors.

13. (Original) The processing core for transposing the matrix of claim 9, wherein the first processing path receives a first sub-instruction and the second processing path receives a second sub-instruction.

14. (Original) The processing core for transposing the matrix of claim 9, wherein each of the first through fourth source registers include a matrix row.

15. (Original) The processing core for transposing the matrix of claim 9, wherein each of the first and second destination registers include a matrix column.

16. (Original) The processing core for transposing the matrix of claim 9, wherein the first and second destination registers are addressed by a first and second sub-instructions which are included in a very long instruction word.

17. (Previously Presented) A method for processing a matrix of elements, the method comprising steps of:

loading a first instruction;

loading a second instruction, wherein the first and second instructions address a first source register, second source register, third source register, fourth source register, first destination register and second destination register;

loading a third instruction;

loading a fourth instruction, wherein the third and fourth instructions address the first source register, the second source register, the third source register, the fourth source register, a third destination register and a fourth destination register;

storing a first element of the first source register in the first destination register; and

storing a fourth element of the first source register in the fourth destination register, wherein a plurality of the first through fourth instructions comprise a same instruction issue.

18. (Original) The method for processing the matrix of elements of claim 17, wherein the first and second instructions include a first operation code and the third and fourth instructions include a second operation code different from the first operation code.

19. (Canceled)

20. (Original) The method for processing the matrix of elements of claim 17, wherein the first instruction is a sub-instruction in a very long instruction word.

21. (Previously Presented) The method for processing the matrix of elements in the processor as recited in claim 1, wherein the location of the first destination and the second destination are expressly specified.

22. (Previously Presented) The method for processing the matrix of elements in the processor as recited in claim 1, wherein the location of the first destination and the second destination are non-adjacent addresses.